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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/785,604
Filing Date: February 16, 2001
Appellant(s): LEE ET AL.

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 8, 2005 appealing from the Office action mailed June 6, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Application Serial No. 09/788,582.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7, 9-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaplinsky (U.S. Patent No. 5,298,866). This rejection is set forth in prior Office Action, Paper No. 20050602, and is reproduced below:

The appellant did not separately argue the dependent claims. There are three independent claims, namely claims 1, 6 and 12: Independent claims 1 and 6 are method claims. Independent claim 12 is an apparatus claim corresponding the method claim. Claim 1 therefore is selected as an exemplary in the rejection below.

Attention to the Board is respectfully directed to Figure 1 and the corresponding description in Kaplinsky.

With respect to claim 1, Kaplinsky teaches:

A method for distributing a clock signal generated by a clock generator (the clock generator which generates the CLOCK signal shown in Fig. 1) to a plurality of nodes [col. 1, lines 6-9] comprising the steps of:

measuring a clock delay for each of said nodes [col. 2, lines 66-67; col. 5, lines 27-28], wherein said clock delay includes clock generator output delays (fanout) [col. 1, line 62 to col. 2, line 2] and resistive-capacitive (RC) delays [col. 2, lines 8-18]; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase [col. 2, line 66 to col. 3, line 2; col. 6, line 53 to col. 7, line 2].

Kaplinsky does not explicitly teach that the clock delay is estimated.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kaplinsky to estimate the clock delay instead of measuring the clock delay because it would allow a faster process of the system.

(10) Response to Argument

In the Appeal Brief, Appellant argued in substances that: (1) Kaplinsky's statement is incorrect; (2) Kaplinsky does not disclose or suggest measuring or estimating a clock delay for each of the nodes; and (3) Kaplinsky does not disclose or suggest adjusting the clock signal based on the estimated clock delay.

(1) Appellant has argued that statements in the Kaplinsky patent, which were relied upon by the examiner in rejecting the claims, are incorrect. The examiner respectfully

disagrees. Appellant's arguments are in essence an allegation that the Kaplinsky patent is invalid. Such allegations are not well taken. An appeal brief before the United States Patent and Trademark Office Board of Patent Appeals and Interferences is not the proper forum for challenging the validity of a U.S. Patent. Moreover, the Appellant's allegations are unsubstantiated and contrary to the plain meaning of the patent. The examiner and those of ordinary skill in the art would not find Kaplinsky's statements in column 6 lines 59-60 to be incorrect. Rather, it is clear to the examiner that when the delay on the signal paths 15 and 29 is large, the phase comparator 63 receives the return signal (input signal 59) *after* receiving the reference signal (input signal 61).

(2) Appellant has argued that Kaplinsky fails to disclose or suggest estimating a clock delay for each of the nodes. The examiner respectfully disagrees. First it is noted that every measurement is only as estimation based on the accuracy of the measuring instrument. Thus, when method disclosed by Kaplinsky calls for measuring a clock delay, that measurement is an estimate of the clock delay.

Kaplinsky clearly discloses measuring a clock delay for each of the nodes. Kaplinsky states in relevant part:

> "the above object has been met with a clock distribution circuit having de-skewing logic at the clock outputs, which senses and measures the clock delay on each signal path and then adjusts the phase of the outgoing clock signals" (column 2, lines 64-66), "Each output driver 11 is connected to receive a clock signal on its input 13 and to transmit the

> clock signal on a conductive wire trace 15, representing an outward signal path, to a clock recipient or load 17" (column 4, lines 49-52), "In order to sense and measure the clock delay on each signal path 15 leading to a clock recipient or load 17, return paths 29 are provided" (column 5, lines 27-29), and "The reference signal used as a basis in measuring the delay on signal paths 15 is derived from a flip-flop 25 from an input clock signal and a DATA signal in the same manner as that used to generate the signal pulse or periodic clock for output by drivers 11" (column 6, lines 26-30).

These statements taken together and considered in the context of Fig. 1 show how clock delay for each of the nodes is calculated. In particular, the clock delay for each node is measured by providing corresponding return path 29 then comparing the return signal on the signal paths 15 and 29 with the reference signal to determine whether the delay is large or small.

(3) Appellant has argued that Kaplinsky fails to disclose or suggest adjusting the clock signal based on the estimated clock delay. The examiner respectfully disagrees. As discussed above, Kaplinsky explicitly discloses adjusting the clock signal based on the estimated clock delay in column 2 at lines 64-66.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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